Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A transceiver front-end, comprising:

a hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port, said hybrid circuit including a series resistance connected between said first port of said hybrid and said third port of said hybrid;

a high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a gain stage, having an input that is connected to an output of said high-pass filter.

2. (Original) The transceiver front-end of claim 1, wherein said input of said gain stage is directly connected to said output of said high-pass filter.

3. (Original) The transceiver front-end of claim 1, said hybrid circuit comprising:

a replica circuit that replicates a transmit signal generated from said transmit source to produce a replica transmit signal that substantially cancels said transmit signal at said third port of said hybrid.

4. (Original) The transceiver front-end of claim 3, wherein said replica transmit signal is substantially 180 degrees out of phase with said transmit signal.

5. (Original) The transceiver front-end of claim 3, wherein said replica circuit comprises a digital-to-analog converter (DAC) that receives transmit data and generates said replica transmit signal.

6. (Canceled)

7. (Currently Amended) The transceiver front-end of claim [[6]] 1, wherein said series resistance is greater than a characteristic impedance of said transmission medium.

8. (Original) The transceiver front-end of claim 7, wherein said series resistance is substantially less than an input impedance of said high-pass filter.

9. (Currently Amended) ~~The transceiver front-end of claim 1, further comprising:~~ A transceiver front-end, comprising:

a hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a high-pass filter, having an input that is directly connected to said third port of said hybrid circuit;

a gain stage, having an input that is connected to an output of said high-pass filter; and

a first digital-to-analog converter (DAC) adapted to receive digital transmit data from said transmit source and having an analog output connected to said first port of said hybrid circuit; ~~and~~

wherein said hybrid circuit comprises a second digital-to-analog converter (DAC) adapted to receive said digital transmit data from said transmit source and having an analog output connected to said third port of said hybrid circuit.

10. (Original) The transceiver front-end of claim 9, said analog output of said second DAC being approximately 180 degrees out of phase with said analog output of said first DAC.

11. (Currently Amended) The transceiver front-end of claim 9, said analog output of said second DAC having an amplitude that is [[a]] scaled by a scaling factor relative to a corresponding amplitude for said analog output of said first DAC.

12. (Original) The transceiver front-end of claim 11, wherein said scaling factor is:

$Rc/(Rc + Rs)$

wherein Rc is a characteristic impedance of said transmission medium and Rs is a series resistance of said hybrid circuit.

13. (Original) The transceiver front-end of claim 1, wherein said high-pass filter has a tunable corner frequency.

14. (Currently Amended) ~~The transceiver front-end of claim 13,~~ A transceiver front-end, comprising:

a hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a gain stage, having an input that is connected to an output of said high-pass filter;

wherein said high-pass filter has a tunable corner frequency; and

wherein said high-pass filter includes a variable resistance that determines said tunable corner frequency.

15. (Original) The transceiver front-end of claim 14, wherein said variable resistance includes:

a first resistor; and

a second resistor that is series-connected with a switch, said second resistor and said switch connected in parallel with said first resistor, said tunable corner frequency adjusted by closing said switch.

16. (Original) The transceiver front-end of claim 1, wherein at least one of said hybrid circuit, said high-pass filter, and said gain stage is differential.

17. (Original) The transceiver front-end of claim 1, wherein each of said hybrid circuit, said high-pass filter, and said gain stage are differential.

18. (Original) The transceiver front-end of claim 1, wherein said gain stage has a constant input impedance.

19. (Canceled)

20. (Currently Amended) ~~The transceiver front-end of claim 19,~~ A transceiver front-end, comprising:

a hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a gain stage, having an input that is connected to an output of said high-pass filter;

wherein said gain stage is a programmable gain stage; and

wherein a gain of said programmable gain stage is tunable in logarithmic steps according to a control signal.

21. (Currently Amended) ~~The transceiver front-end of claim 19, wherein said programmable gain stage comprises:~~ A transceiver front-end, comprising:

a hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a gain stage, having an input that is connected to an output of said high-pass filter;

wherein said gain stage is a programmable gain stage including,

a resistor ladder having multiple taps, each tap having a corresponding switch connected to an output of said programmable gain stage; and

one or more parallel resistors connected from said resistor ladder to a virtual ground.

22. (Original) The transceiver front-end of claim 1, wherein said hybrid circuit, said high-pass filter, and said gain stage are passive.

23. (Original) The transceiver front-end of claim 1, wherein said third port of said hybrid circuit is substantially isolated from said transmit source, despite variations in an input impedance of said high-pass filter.

24. (Canceled)

25. (Currently Amended) The transceiver front-end of claim [[24]] 26, wherein said differential hybrid circuit, said differential high-pass filter, and said differential gain stage are passive.

26. (Currently Amended) ~~The transceiver front-end of claim 24, further comprising:~~ A transceiver front-end, comprising:

a differential hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a differential high-pass filter, having an input that is directly connected to said third port of said hybrid circuit;

a differential programmable gain stage, having an input that is directly connected to an output of said high-pass filter; and

a first digital-to-analog converter (DAC) adapted to receive digital transmit data from said transmit source and having an analog output connected to said first port of said hybrid circuit;

wherein said differential hybrid circuit includes,

a series resistance between said first port and said third port; and

a second digital-to-analog converter (DAC) adapted to receive said digital transmit data from said transmit source and having an analog output connected to said third port of said hybrid circuit, wherein said analog output of said second DAC cancels said analog output from said first DAC at said third port of said hybrid circuit.

27. (Original) The transceiver front-end of claim 26, wherein said analog output signal of said second DAC is approximately 180 degrees out of phase with said analog output signal from said first DAC.

28. (Original) The transceiver front-end of claim 26, said analog output of said second DAC being scaled by a scaling factor relative to said analog output of said first

DAC, said scaling factor determined by Rc/(Rc + Rs), wherein Rc is a characteristic impedance of said transmission medium and Rs is a series resistance of said hybrid circuit.

29. (Currently Amended) ~~The transceiver front-end of claim 24,~~ A transceiver front-end, comprising:

a differential hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a differential high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a differential programmable gain stage, having an input that is directly connected to an output of said high-pass filter;

wherein said high-pass filter comprises:

a series capacitor; and

a variable resistance connected in-series with said series capacitor, wherein a corner frequency of said high-pass filter is tuned by adjusting said variable resistance.

30. (Currently Amended) ~~The transceiver front-end of claim 24,~~ A transceiver front-end, comprising:

a differential hybrid circuit having a first port that is connectable to a transmission medium, a second port that is connectable to a transmit source, and a third port;

a differential high-pass filter, having an input that is directly connected to said third port of said hybrid circuit; and

a differential programmable gain stage, having an input that is directly connected to an output of said high-pass filter;

wherein said programmable gain stage comprises:

a resistor ladder having multiple taps, each tap having a corresponding switch connected to an output of said programmable gain stage; and

one or more parallel resistors connected from said resistor ladder to a virtual ground.